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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,741	09/29/2003	Kalyan Muthukumar	884.890US1	1924

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EXAMINER	
TECKLU, ISAAC TUKU	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,741	MUTHUKUMAR, KALYAN	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-10,12-15,19-25 and 27-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-10, 12-15, 19-25 and 27-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on 01/22/2007.
2. Claims 7, 10, 12, 14, 18, 21, 27 and 30 have been amended.
3. Claims 1-6, 11, 16-17 and 26 have been cancelled.
4. Claims 7-10, 12-15, 19-25 and 27-32 have been reexamined.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 7-10, 12-15, 19-25 and 27-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Thompson (U.S. 2003/0237080 A1).

Per claim 7 (Currently Amended), Thompson discloses a method of software pipelining for improving efficiency of loop handling, the method (paragraph [0015] "... register allocation and software pipelining...") comprising:

checking for availability of rotating registers to hold computed values that are live across multiple stages in a software-pipelined loop (paragraph [0052] "... determine when to spill the contents of specific rotating registers to a memory device ..."); and

spilling and filling the computed values held in rotating registers in a software-pipelined loop using rotating stack memory locations for rotating registers (paragraph [0014] "... the contents of the spilled registers are temporarily moved to RAM ..."), when there are no rotating registers available to hold the computed values (paragraph [0053] and e.g. FIG. 6B, spiller 640

and related text), wherein the number of the rotating stack memory locations used for spilling and filling the computed values is equal to the number of simultaneous live values generated by the rotating register (paragraph [0055] "... live ranges are less or equal to the initial interval...").

Per claim 8, Thompson discloses the method of claim 7, wherein the computed values are Floating Point (FP) values (paragraph [0010] "... processing a floating-point ...").

Per claim 9, Thompson discloses the method of claim 7, wherein the rotating registers are FP rotating registers (paragraph [0010] "... processing a floating-point ..." and e.g. FIG. 6A and related text).

Per claim 10 (Currently Amended), Thompson discloses a method of software pipelining for improving efficiency of loop handling, the method comprising:

checking for availability of FP rotating registers to hold FP computed values that are live across multiple stages in a software-pipelined loop (paragraph [0052] "... determine when to spill the contents of specific rotating registers to a memory device ..."); and

spilling and filling the computed values using rotating integer registers for holding addresses of stack memory locations when there are no FP rotating registers available to hold the computed value (e.g. FIG. 6B, 660 and related text).

Per claim 12 (Currently Amended), Thompson discloses the method of claim [[11]] 10, wherein spilling and filling the computed value comprises:

storing the computed value in the stack memory locations whose addresses are held in corresponding N+1 rotating integer registers (paragraph [0046] "... stores values of common ... "); and

loading from the stack memory locations whose addresses are held in corresponding N+1 rotating integer registers based on number of stages between when the loading occurs from the storing of the corresponding computed value (paragraph [0053] "... inputs and forwards ... ").

Per claim 13, Thompson discloses the method of claim 10, wherein target registers for filling could be any available FP registers (e.g. FIG. 6B, element 652 and related text).

Per claim 14 (Currently Amended), Thompson discloses a method of software pipelining for improving efficiency of loop handling, the method comprising using post-incremented memory operations for spilling and filling of live computed values, held in a FP rotating register (paragraph [0052] "... determine when to spill the contents of specific rotating registers to a memory device ..."), that are live across multiple stages in a software-pipelined loop, using non-rotating registers, when there are no rotating integer registers (e.g. FIG. 6B, 662 STATIC REGISTER IR and related text) available to hold rotating stack memory locations (e.g. FIG. 6B and related text).

checking for availability of N+1 non-rotating integer registers available for spilling and filling, wherein N is a number of stages a computed value that needs to be spilled is live in the software-pipelined loop (paragraph [0052] "... determine when to spill the contents of specific rotating registers to a memory device ..."); and

spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 non-rotating integer registers, when the N+1 non-rotating registers are available (paragraph [0053] and e.g. FIG. 6B, spiller 640 and related text).

Per claim 15, Thompson discloses the method of claim 14, wherein using the non-rotating registers comprises: using the non-rotating integer registers (e.g. FIG. 6B, 662 STATIC REGISTER IR and related text).

Per claim 18 (Currently Amended), Thompson discloses a method of software pipelining efficiency of loop handling, the method comprising spilling and filling of live computed values, held in a rotating register, that are live across multiple stages in a software-pipelined loop, using two non-rotating integer registers (paragraph [0053] and e.g. FIG. 6B, spiller 640 and related text), when there are no FP rotating registers available and when there are no rotating integer registers available for holding rotating stack memory locations, and when there are not enough

non-rotating integer registers available for holding rotating stack memory locations (paragraph [0055] "... live ranges are less or equal to the initial interval...").

Per claim 19, Thompson discloses the method of claim 18, wherein the two non-rotating registers do not have to be contiguous (e.g. FIG. 6B and related text).

Per claim 20, Thompson discloses the method of claim 18, wherein the rotating stack memory locations have to be contiguous and in descending order (e.g. FIG. 6A-B and related text).

Per claim 21 (Currently Amended), Thompson discloses a method of software pipelining for improving efficiency of loop handling, the method comprising: checking for availability of rotating integer registers and non-rotating integer registers, to spill and fill computed values held in a FP rotating register, that are live across multiple stages in a software-pipelined loop;

spilling and filling the computed values, held in a FP rotating register, using the rotating integer registers to hold [[the]] rotating stack memory locations, when there are no FP rotating registers available to hold the computed values (paragraph [0053] and e.g. FIG. 6B, spiller 640 and related text);

spilling and filling the computed values, held in the FP rotating register, using the non-rotating registers to hold [[the]] rotating stack memory locations, when there are no FP rotating registers to hold the computed values and further when there are no rotating integer registers available for holding rotating stack memory locations (paragraph [0052] "... static register allocator and spiller ..."); and

spilling and filling the computed values held in the FP rotating register, using two non-rotating integer registers to hold the rotating stack memory locations, when there are no FP rotating registers to hold the computed values, where there are no rotating integer registers available, and further when there are only a few non-rotating integer registers available for holding rotating stack memory locations (paragraph [0053] "... static register allocator and memory spiller 660 of FIG. 6B ...").

Per claim 22, Thompson discloses the method of claim 21, wherein spilling and filling the computed values using the rotating integer registers comprises:

checking for availability of N+1 rotating integer registers, wherein N is number of stages a computed value that needs to be spilled is live in the software-pipelined loop (paragraph [0052] "... determine when to spill the contents of specific rotating registers to a memory device ..."); and

spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 rotating integer registers, when the N+1 rotating integer registers are available (paragraph [0053] and e.g. FIG. 6B, spiller 640 and related text).

Per claim 23, Thompson discloses the method of claim 21, wherein spilling and filling the computed values using non-rotating integer registers comprises:

checking for availability of N+1 non-rotating integer registers available for spilling and filling, wherein N is a number of stages a computed value that needs to be spilled is live in the software-pipelined loop (paragraph [0052] "... determine when to spill the contents of specific rotating registers to a memory device ..."); and

spilling and filling the computed values in stack memory locations whose addresses are held in corresponding N+1 non-rotating integer registers, when the N+1 non-rotating registers are available (e.g. FIGURE 9C and related text).

Per claim 24, Thompson discloses the method of claim 21, wherein the two non-rotating registers do not have to be contiguous (paragraph [0053] and e.g. FIG. 6B, spiller 640 and related text).

Per claim 25, Thompson discloses the method of claim 21, wherein the rotating stack memory locations have to be contiguous and in descending order (e.g. FIG 6A and related text).

Per claim 27, this is the article version of the claimed method discussed above (Claim 21), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Thompson.

Per claim 28, this is the article version of the claimed method discussed above (Claim 22), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Thompson.

Per claim 29, this is the article version of the claimed method discussed above (Claim 23), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Thompson.

Per claim 30, this is the system version of the claimed method discussed above (Claim 21), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Thompson.

Per claim 31, this is the system version of the claimed method discussed above (Claim 22), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Thompson.

Per claim 32, this is the system version of the claimed method discussed above (Claim 23), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, this claim is also anticipated by Thompson.

Response to Arguments

7. Applicant's arguments with respect to claims 7-10, 12-15, 19-25 and 27-32 have been considered but are moot in view of the new ground(s) of rejection. See Thompson art made of record.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER